Claims:

Sub A5

1. An apparatus comprising:

a memory array having a first portion and a second portion, the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor and the second portion of the memory array is accessible only by a second processor.

2. The apparatus of claim 1, wherein the memory array comprises a third portion that is different than the first portion and the second portion, wherein the third portion of the memory array is accessible by both the first processor and the second processor.

3. The apparatus of claim 1, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal.

4. The apparatus of claim 3, wherein the first portion and the second portion of the memory array are coupled to a same power supply potential.

5. The apparatus of claim 1, wherein the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory

array depending on an operational load of the first processor or the second processor.

6. The apparatus of claim 5, wherein the memory array is further adapted to increase the size of the first portion and decrease the size of the second portion due to an increase in the operational load of the first processor.

7. The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array substantially simultaneously as the second processor accesses the second portion of the memory array.

8. The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may read the first portion of the memory array as the second processor writes to the second portion of the memory array.

9. The apparatus of claim 1, wherein the memory array comprises memory selected from the group consisting of static random access memory, dynamic random access memory, read only memory, electrically erasable and programmable read only memory, and flash memory.

10. An apparatus comprising:

a memory array having a first portion and a second portion;

a first processor; and

a second processor, wherein the first portion of the memory array is accessible only by the first processor, and the second portion of the memory array is accessible only by the second processor.

11. The apparatus of claim 10, further comprising:

a first bus to couple the first processor to the first portion of the memory array; and

a second bus to coupled the second processor to the second portion of the memory array.

12. The apparatus of claim 10, wherein the memory array comprises a first port and a second port, the first port coupling the first portion of the memory array to the first processor and the second port coupling the second portion of the memory array to the second processor.

13. The apparatus of claim 10, further comprising a bus to couple the first processor and the second processor to the memory array.

14. The apparatus of claim 13, wherein the memory array further comprises a collision detector to arbitrate access to the first portion and the second portion of the memory array by the first processor and the second processor.

15. The apparatus of claim 10, further comprising:

a memory controller coupled to the first processor and the second processor; and

a bus to couple the memory controller to the memory array.

16. The apparatus of claim 10, wherein the memory array comprises a third portion that is different than the first portion and the second portion, wherein the third portion of the memory array is accessible by both the first processor and the second processor.

17. The apparatus of claim 10, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal and a same power supply potential.

18. The apparatus of claim 10, wherein the memory array is adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second

processor.

19. The apparatus of claim 10, wherein the memory array is adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor and the second processor.

20. The apparatus of claim 10, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array substantially simultaneously as the second processor accesses the second portion of the memory array.

21. The apparatus of claim 10, wherein the memory array comprises static random access memory.

22. A system comprising:

a first processor;

a second processor;

a memory bus;

a memory array, wherein the first processor and the second processor are coupled to the memory array by the memory bus; and

an arbitrator to resolve access conflicts to the memory array by the first processor and the second processor.

23. The system of claim 22, wherein the memory array comprises a first portion and a second portion, the first portion of the memory array being accessible only by the first processor and the second portion of the memory array being accessible only by the second processor.

24. The system of claim 23, wherein the memory array comprises a third portion that is accessible by both the first processor and the second processor.

25. The system of claim 23, wherein the arbitrator is adapted to permit the first processor to read the first portion of the memory array as the second processor writes to the second portion of the memory array.

26. The system of claim 23, wherein the arbitrator is adapted to permit the first processor to read the first portion of the memory array as the second processor read to the second portion of the memory array.

27. The system of claim 23, wherein the arbitrator is located within the memory array.

28. The system of claim 22, wherein the memory bus comprises a chip select line to indicate which of the first processor and the second processor has initiated an access of the memory array.

29. The system of claim 22, wherein the arbitrator is adapted to decode which of the first processor and the second processor has initiated an access of the memory array.

30. A method comprising:

increasing a first amount of a memory array that is accessible only by a first processor while reducing a second amount of memory array that is accessible only by a second processor.

31. The method of claim 30, further comprising:

accessing a third amount of the memory array with the first processor; and

accessing the third amount of the memory array with the second processor.

32. The method of claim 30, further comprising arbitrating an access conflict to the memory array between the first processor and the second processor.

33. The method of claim 30, further comprising writing to the first amount of the memory array while reading the second portion of the memory array with the second processor.

34. The method of claim 33, wherein writing the first amount of the memory array occurs substantially simultaneous with reading the second portion of the memory array with the second processor.